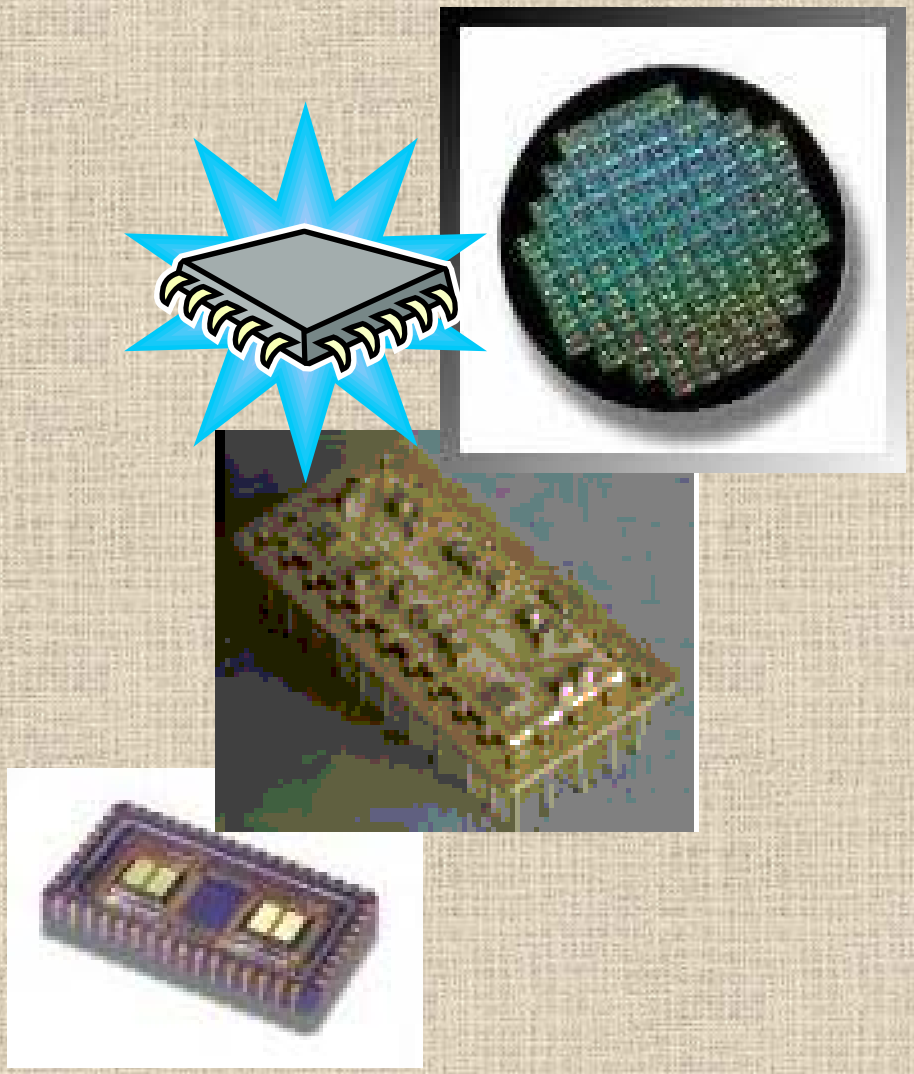
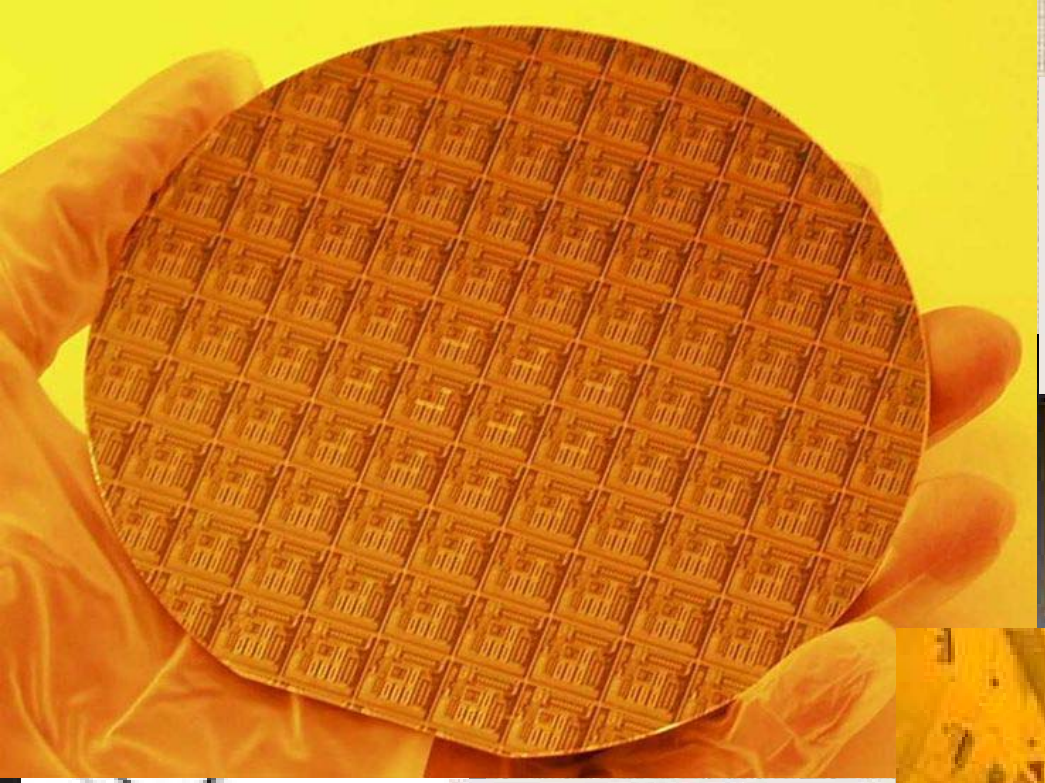
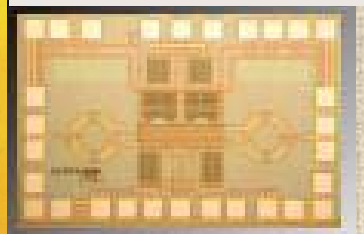
Fabricación de Circuitos Integrados



María Isabel Schiavon - 2006

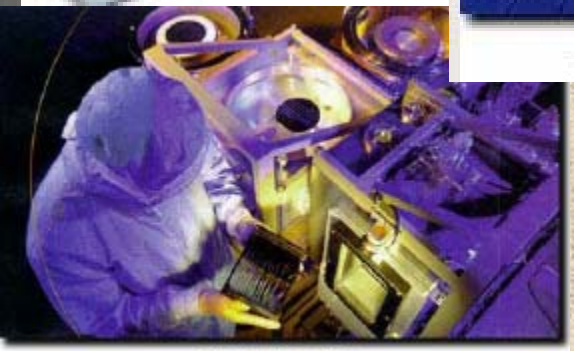


Polysilicon Ingots

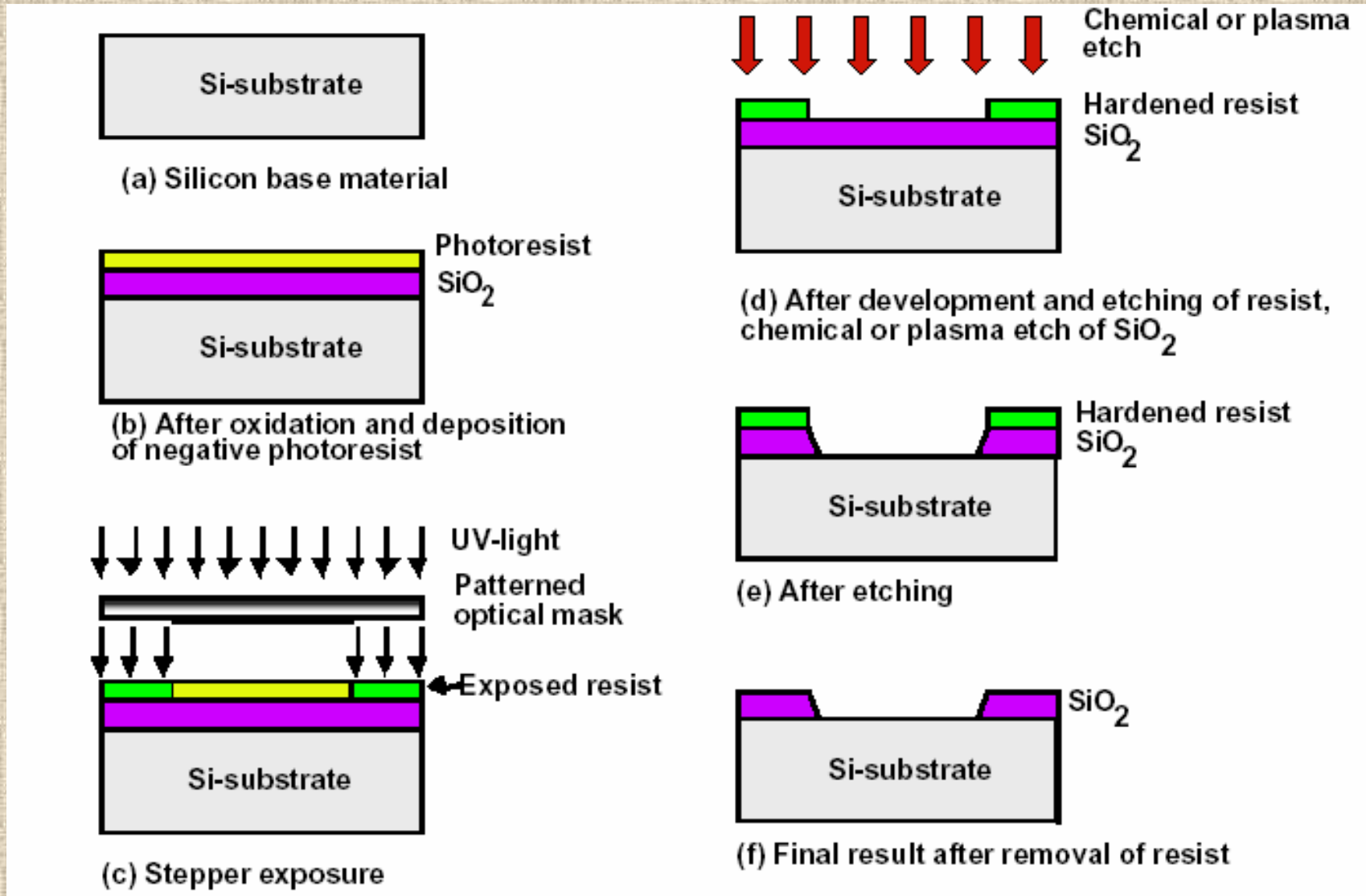


PVD Sputtering Tool
(Sputtered Films Corporation)

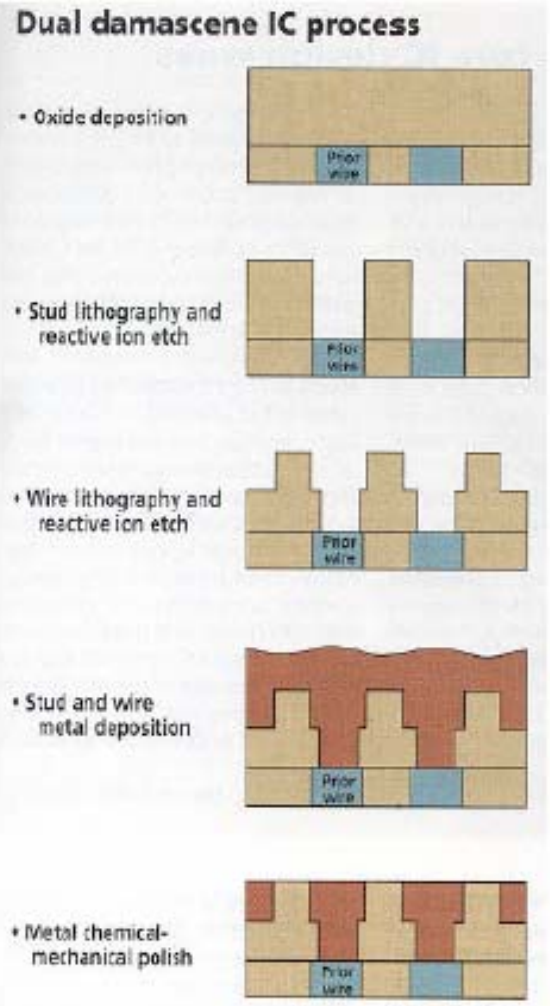
Ion Implanter
(Varian Associates)



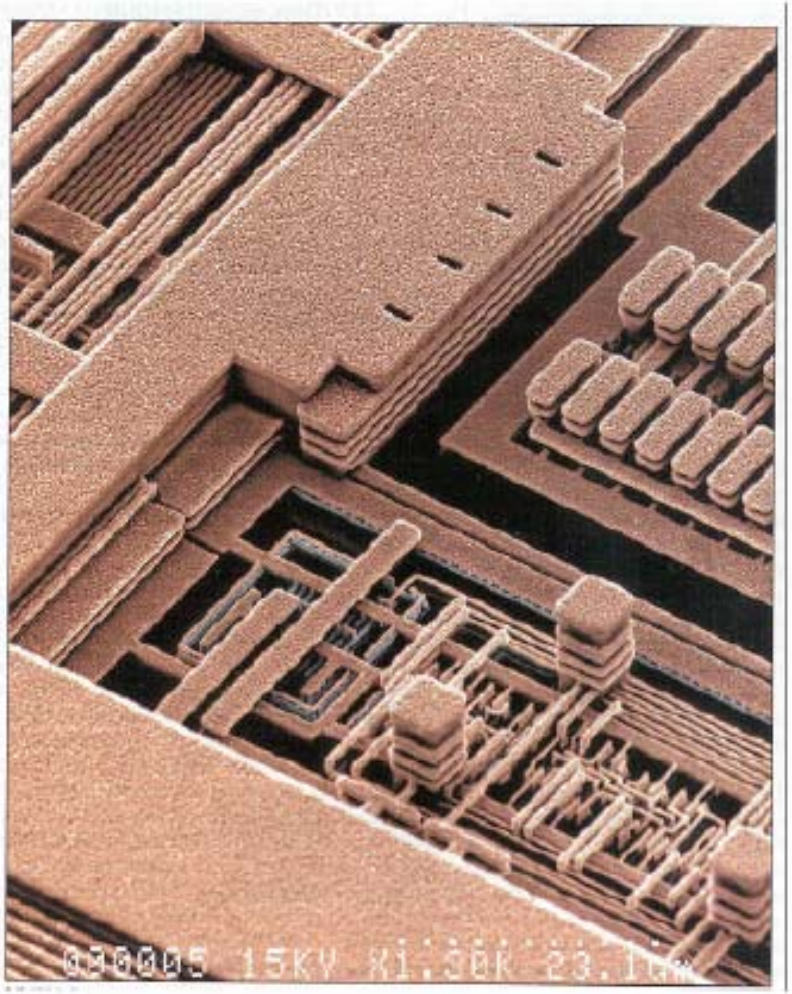
Thin Film Deposition
(Alcatel High Vacuum Technology)


Si-substrate
(a) Silicon base material
Photoresist
SiO_2
Si-substrate
(b) After oxidation and deposition of negative photoresist
UV-light
Patterned optical mask
Exposed resist
Si-substrate
(c) Stepper exposure
Chemical or plasma etch
Hardened resist
SiO_2
Si-substrate
(d) After development and etching of resist, chemical or plasma etch of SiO_2
Hardened resist
SiO_2
Si-substrate
(e) After etching
SiO_2
Si-substrate
(f) Final result after removal of resist

Dual damascene IC process



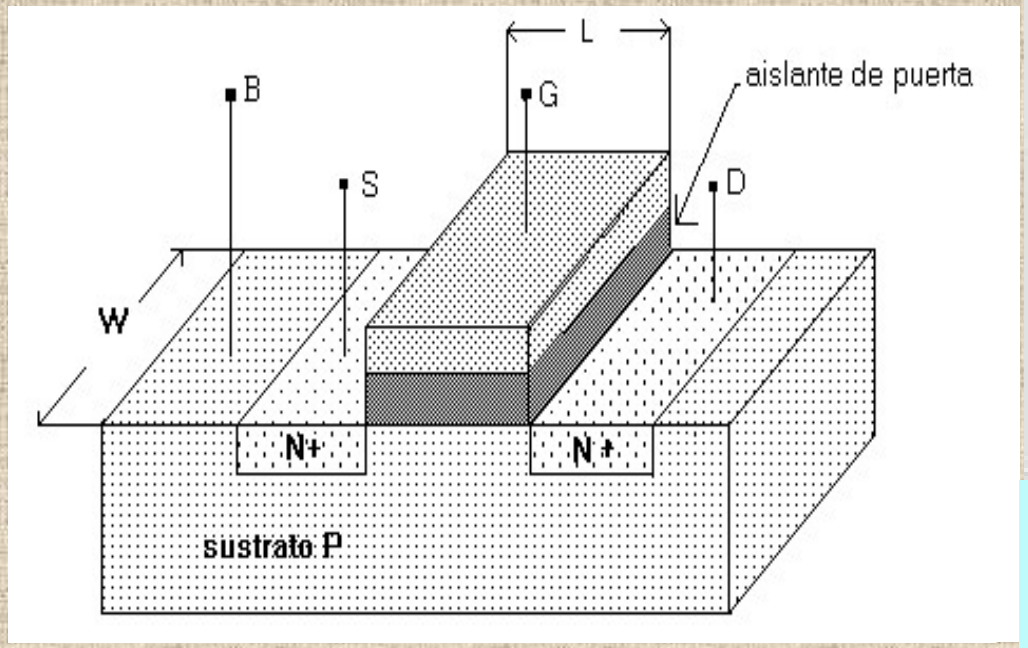
Source: IBM Corp.



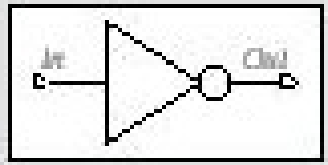
El Proceso Tecnológico

CMOS

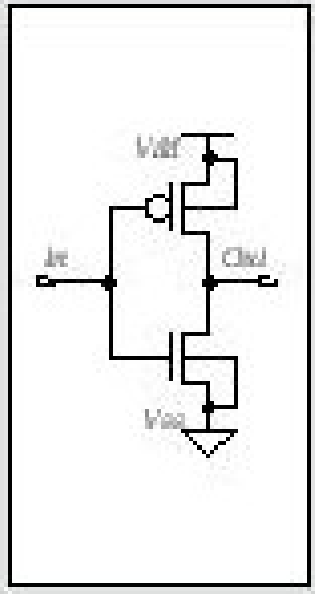
La tecnología más popular

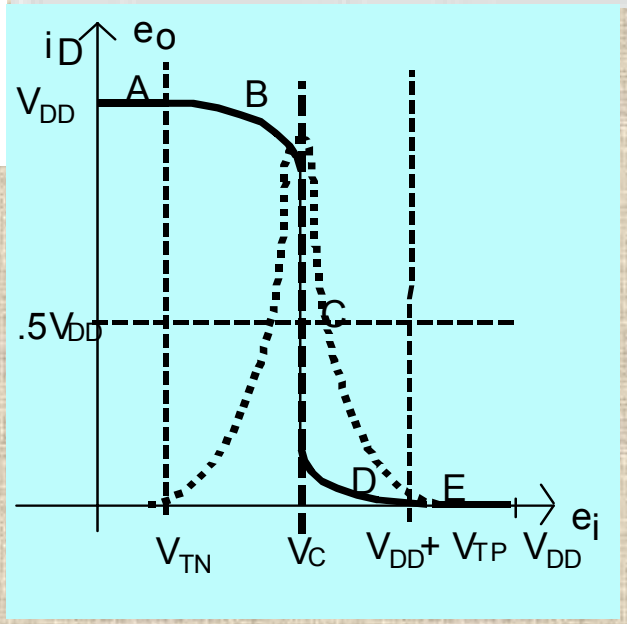


$Out = \overline{In}$

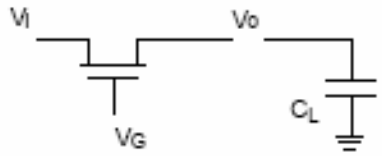


In	Out
0	1
1	0





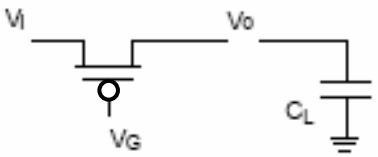
- Simplicidad de diseño
- Baja disipación
- Altos niveles de integración



$V_G=V \Rightarrow$ NMOS conduce

Si $V_i=0$ (source) $\Rightarrow$
C se descarga totalmente
Si $V_i=V$ (drain) $\Rightarrow$
C se carga hasta $V_C=V-V_T$

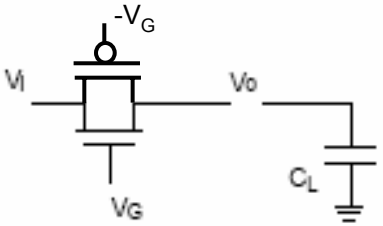
$V_G=0 \Rightarrow$ NMOS cortado



$V_G=0 \Rightarrow$ PMOS conduce

Si $V_i=V$ (source) $\Rightarrow$
C se carga totalmente ($V_C=V$)
Si $V_i=0$ (drain) $\Rightarrow$
C se descarga hasta $V_C=V_T$

$V_G=V \Rightarrow$ PMOS cortado



Puerta de Transmisión

Los dos transistores conducen al mismo tiempo

Inversor CMOS

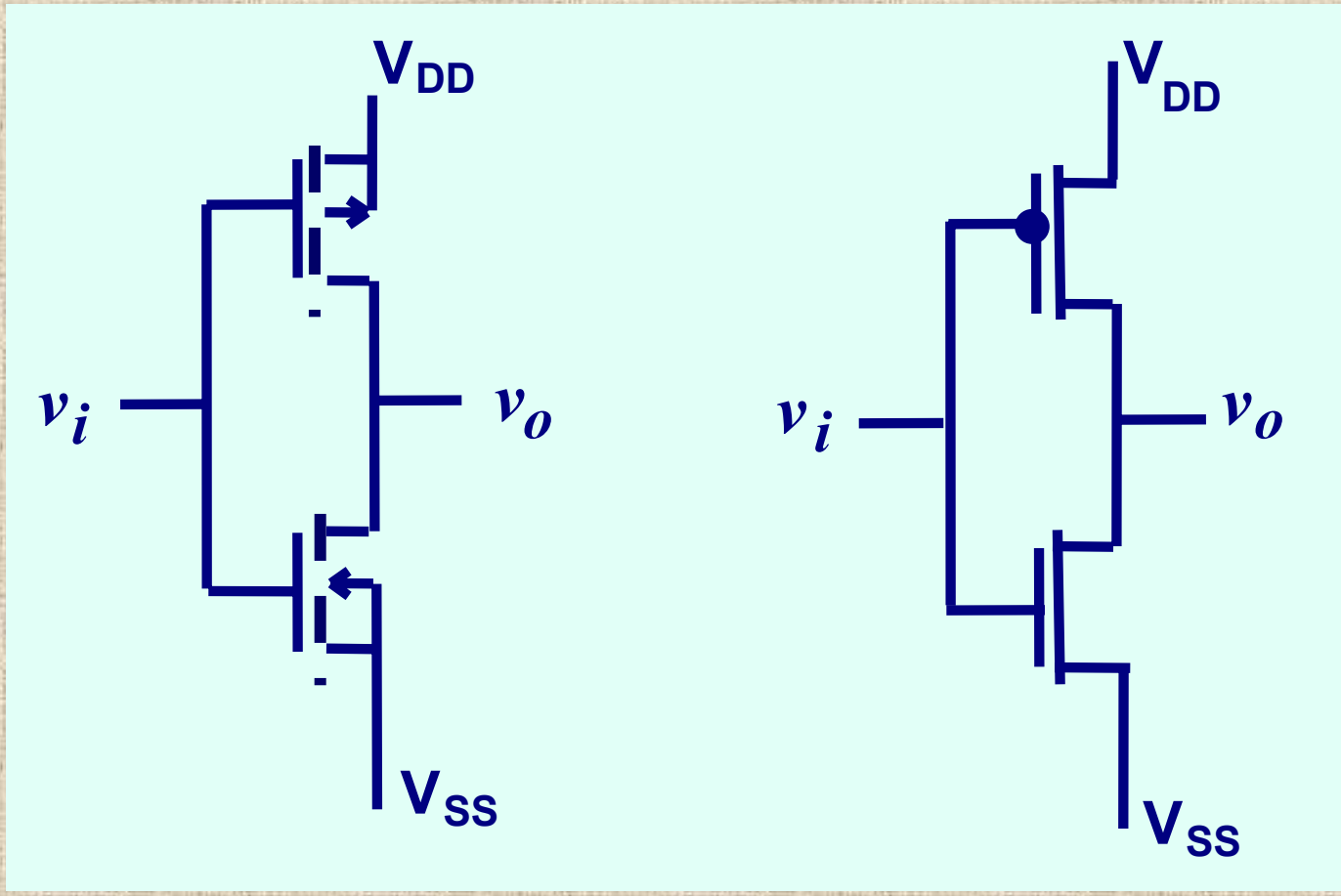
$v_i = v_{GS_N}$

$v_{DS_N} = v_o$

$V_{T_N} > 0$

$V_{T_P} < 0$

$V_{SS} \leq 0$



$v_{GS_P} = v_i - V_{DD}$

$v_{DS_P} = v_{DS_N} - V_{DD}$

$i_{D_N} = -i_{D_P}$

$v_i = v_{GS_N} < V_{T_N}$

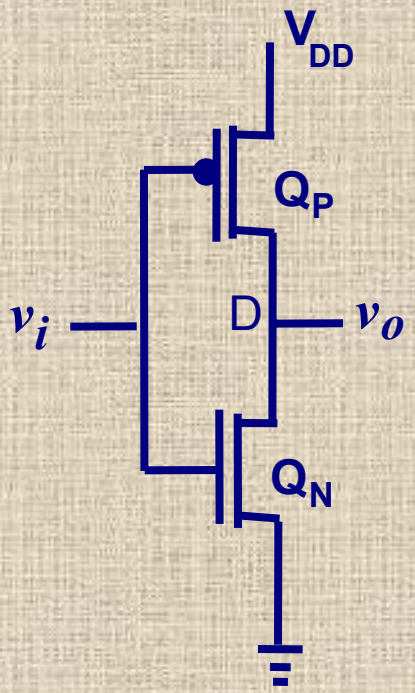
Q_n *cortado*

$v_{DS_N} = v_o \approx V_{DD}$

$v_{GS_P} = v_i - V_{DD} < V_{T_P} < 0$

Q_p *conduce*

zona corriente constante



$v_{GS_N} > V_{T_N}$ Q_n *conduce*

$v_{DS_N} > v_{GS_N} - V_{T_N}$

Q_n *zona cte. cte.*

$v_{DS_N} < v_{GS_N} - V_{T_N}$

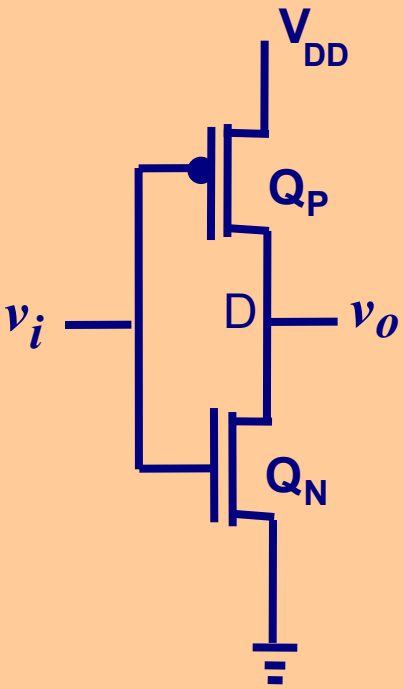
Q_n *zona resistiva*

$v_{GS_P} = v_i - V_{DD}$

$v_{DS_P} = v_o - V_{DD}$

$|v_{DS_P}| > |v_{GS_P} - V_{T_P}|$ *zona cte. cte.*

$|v_{DS_P}| < |v_{GS_P} - V_{T_P}|$ *zona resistiva*



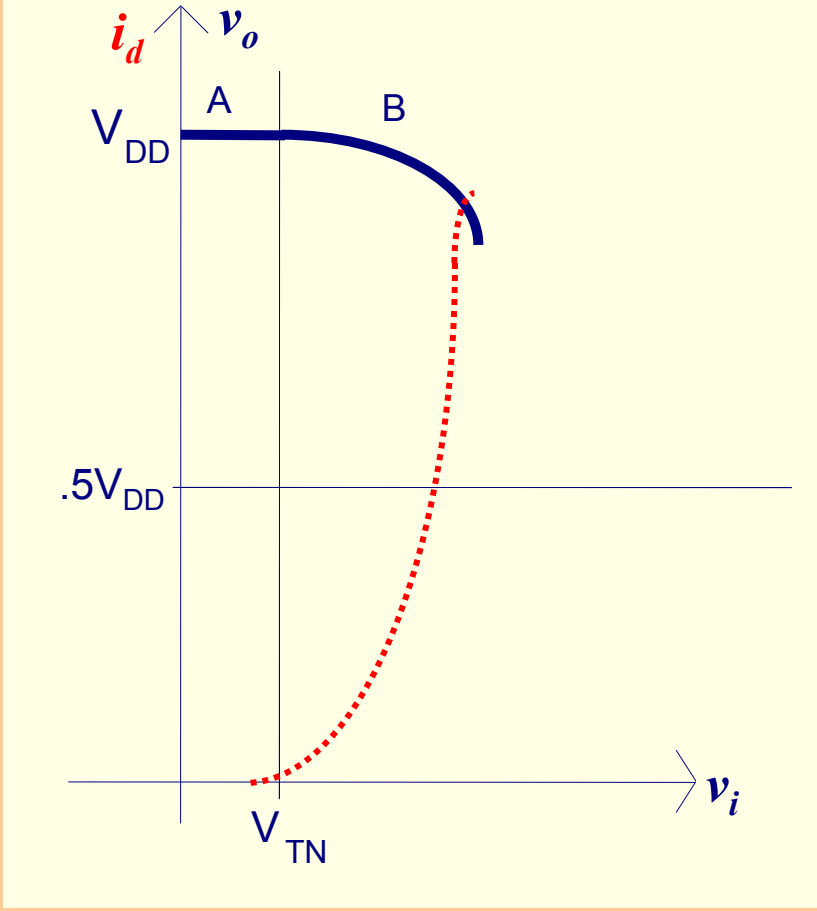
$v_i < V_{T_N}$

zona A

$$\left|v_{DS_P}\right| < \left|v_{GS_P} - V_{T_P}\right|$$

Q_n corte

Q_p zona resistiva



zona B

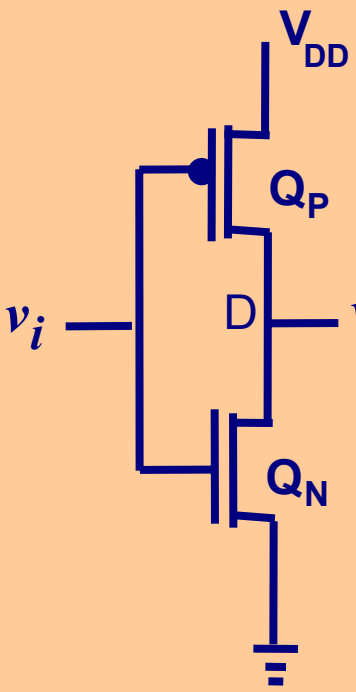
$v_i \geq V_{T_N}$

$$\left|v_{DS_N}\right| > \left|v_{GS_N} - V_{T_N}\right|$$

$$\left|v_{DS_P}\right| < \left|v_{GS_P} - V_{T_P}\right|$$

Q_n zona cte. cte.

Q_p zona resistiva



zona C

$$v_i \geq V_{T_N}$$

$$\left|v_{DS_N}\right| > \left|v_{GS_N} - V_{T_N}\right|$$

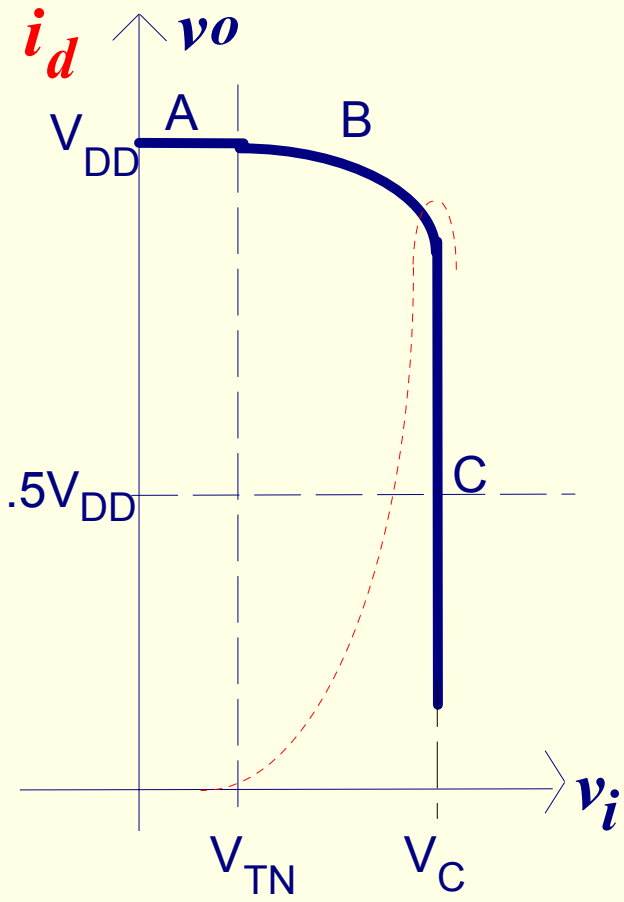
$$\left|v_{DS_P}\right| > \left|v_{GS_P} - V_{T_P}\right|$$

Q_n y Q_p zona cte. cte.

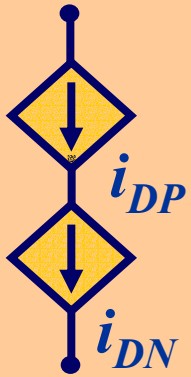
$$i_{DS_N} = -i_{DS_P}$$

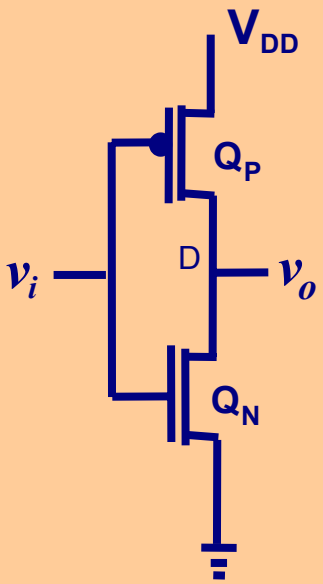
$$\frac{\beta_N}{2}\left(v_i - V_{T_N}\right)^2 = \frac{\beta_P}{2}\left(v_i - V_{DD} - V_{T_P}\right)^2$$

$$v_i = \left(V_{DD} + V_{T_P} + V_{T_N}\sqrt{\frac{\beta_N}{\beta_P}}\right)\left(1 + \sqrt{\frac{\beta_N}{\beta_P}}\right)^{-1} = V_C$$



Dos fuentes de corriente en serie



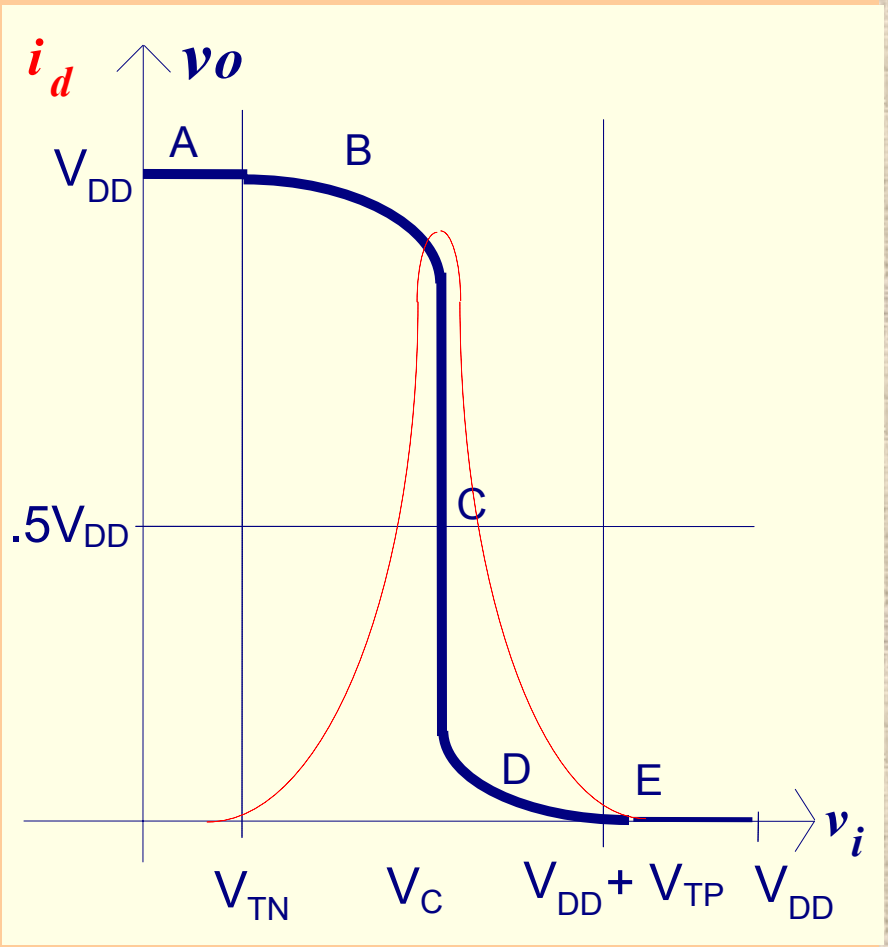


zona D

$$\left|v_{DS_N}\right| < \left|v_{GS_N} - V_{T_N}\right|$$

Q_n zona resistiva

Q_p zona cte. cte



zona E

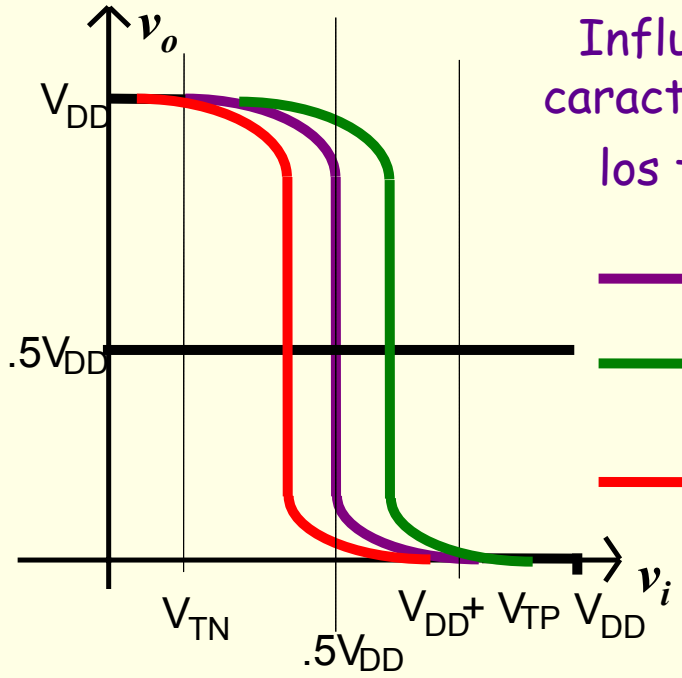
$$v_i \geq V_{DD} - \left|V_{T_P}\right|$$

$$\left|v_{DS_P}\right| > \left|v_{GS_P} - V_{T_P}\right|$$

$$\left|v_{DS_N}\right| < \left|v_{GS_N} - V_{T_N}\right|$$

Q_n zona resistiva

Q_p cortado



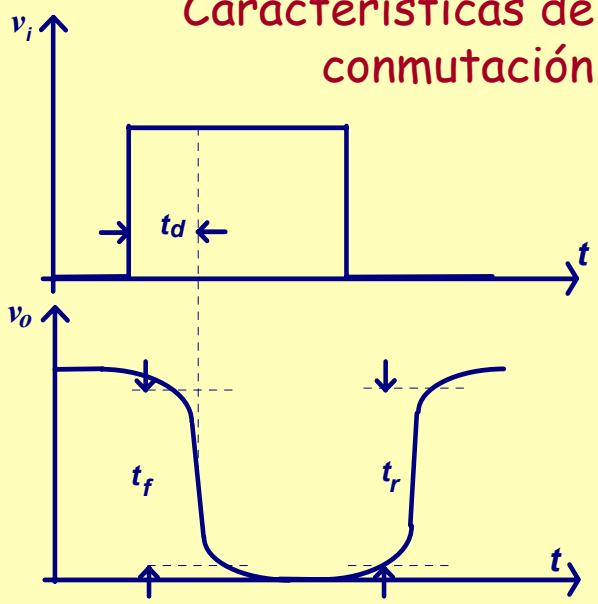
Influencia de las características de los transistores

$\beta_N / \beta_P = 1$

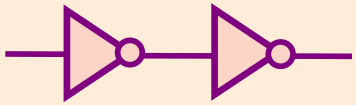
$\beta_N / \beta_P = 0{,}1$

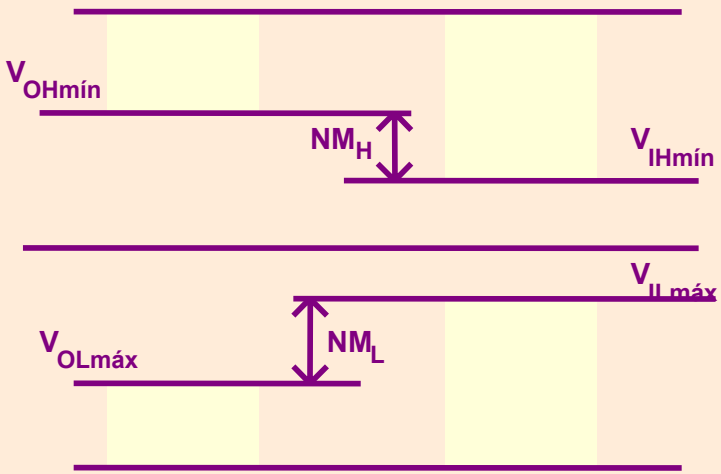
$\beta_N / \beta_P = 10$

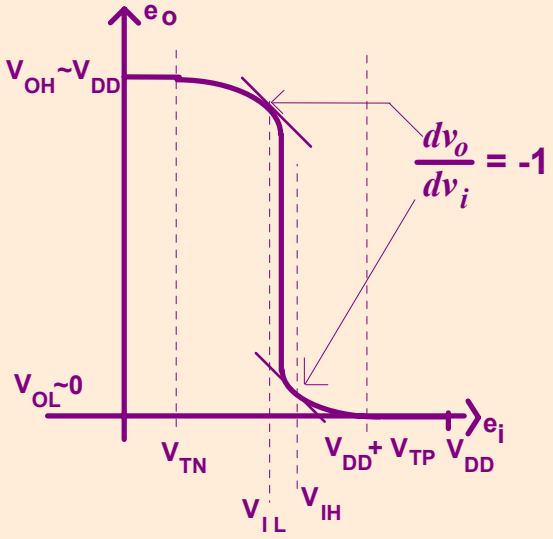
Características de conmutación



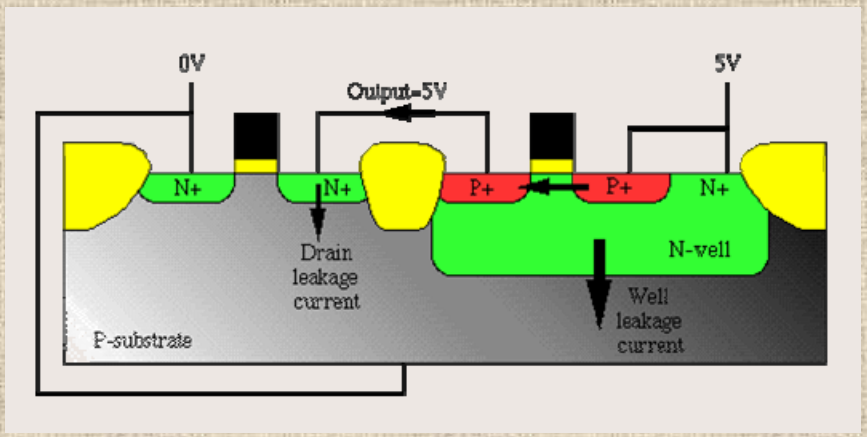
Margen de ruido



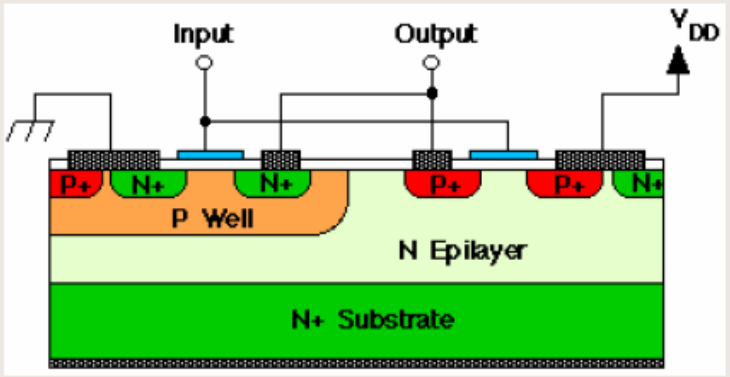




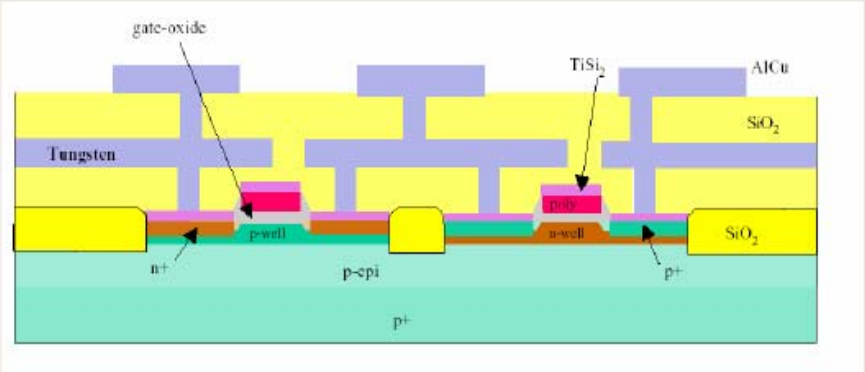
Proceso Pozo N



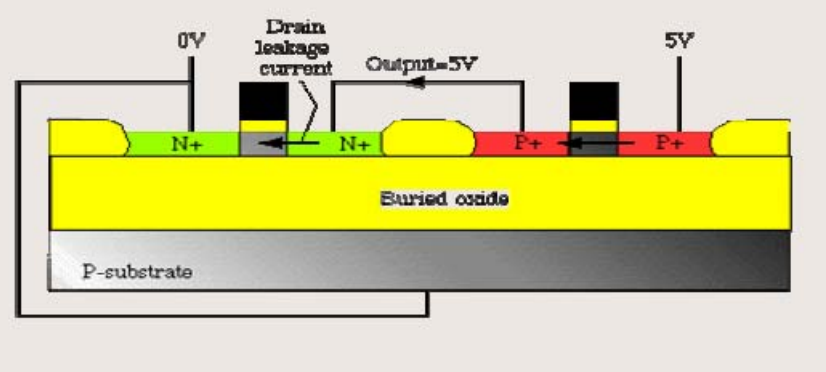
Proceso Pozo P



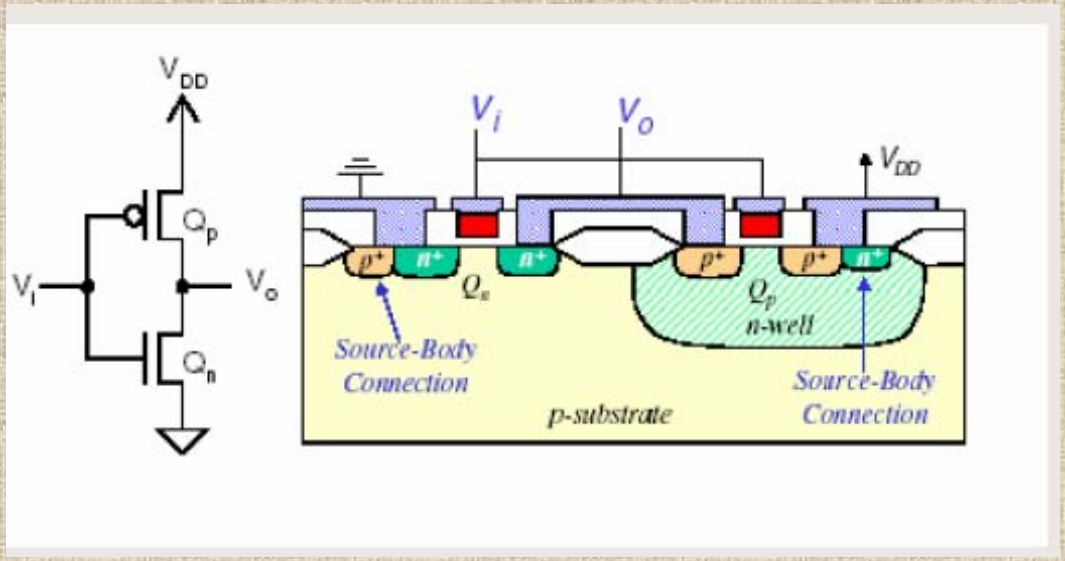
Proceso Doble Pozo



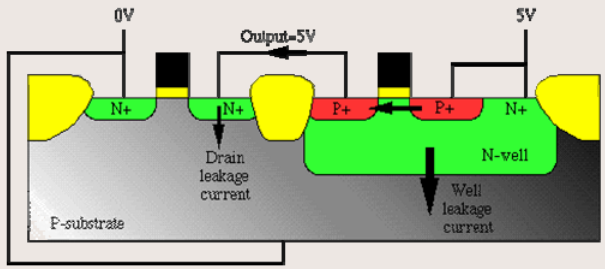
Proceso SOI



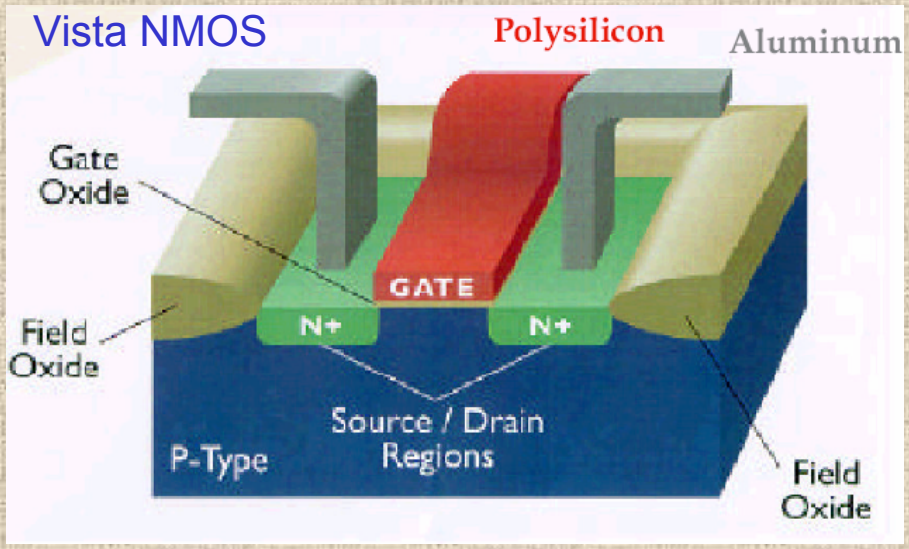
Sección inversor CMOS



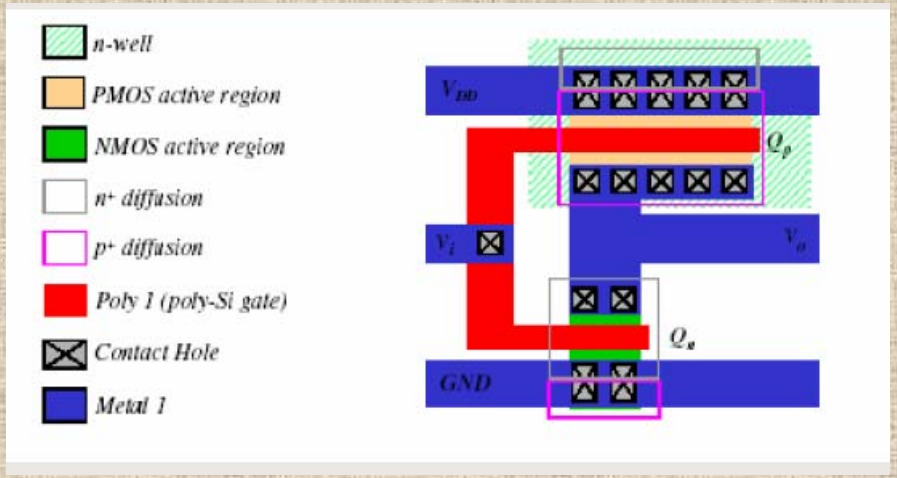
Proceso Pozo N



Vista NMOS

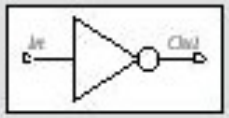


Layout inversor CMOS

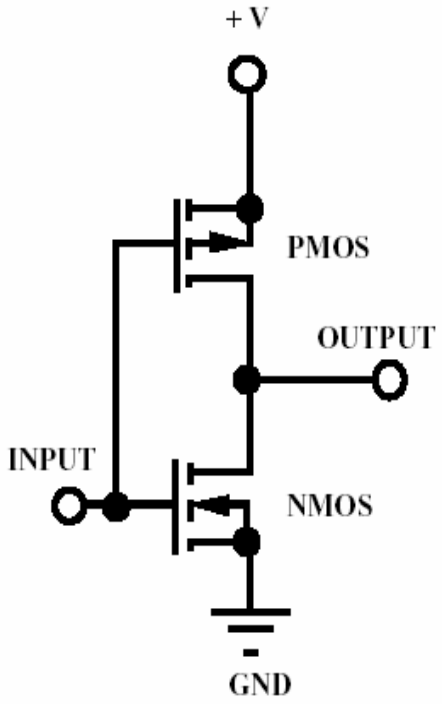


Inversor CMOS

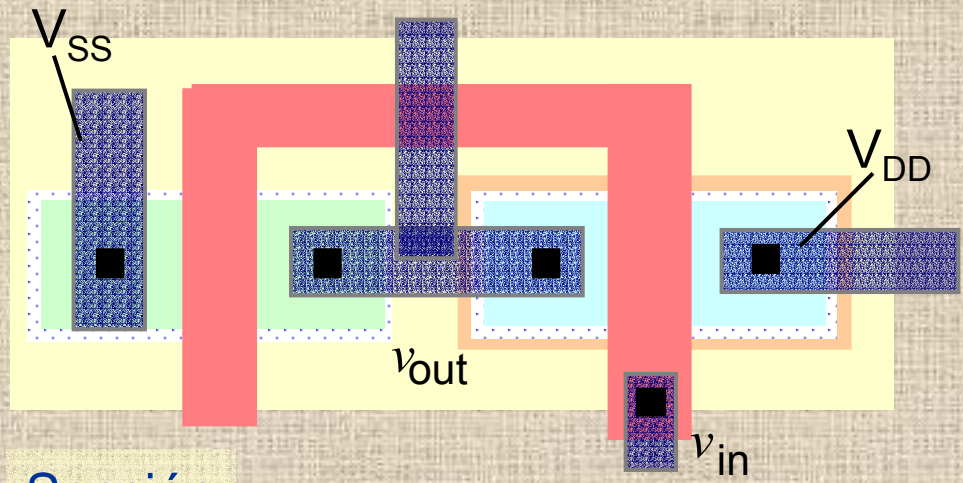
Out = $\overline{\text{In}}$



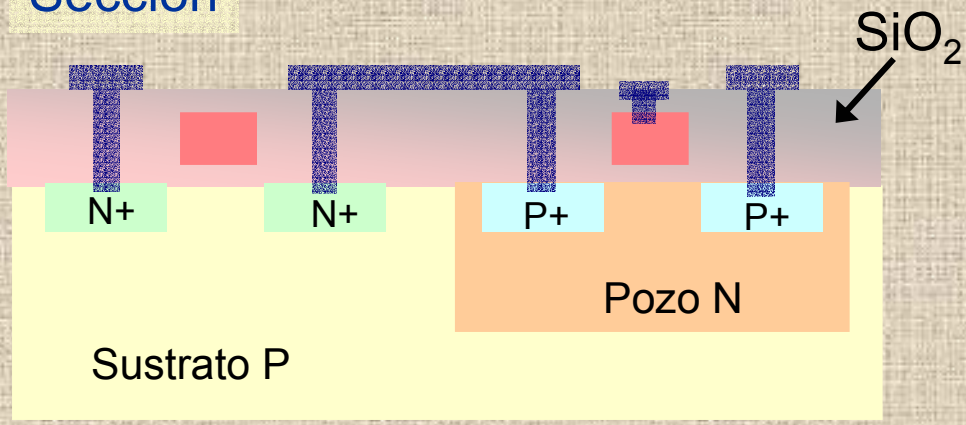
In	Out
0	1
1	0



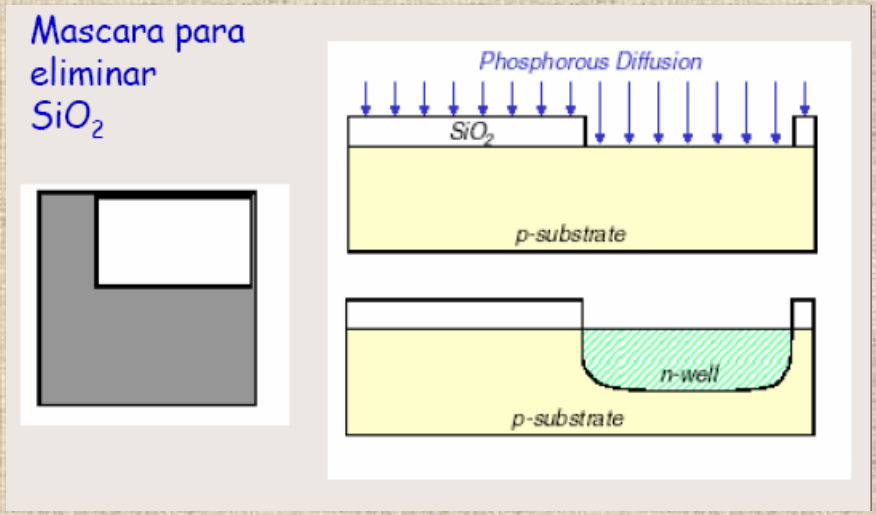
Layout



Sección



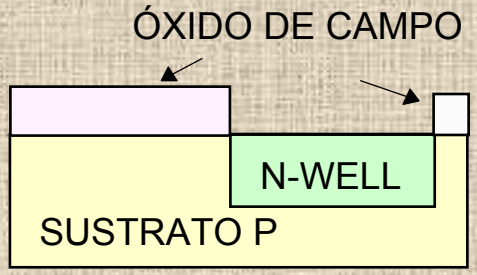
CMOS: etapas proceso fabricación

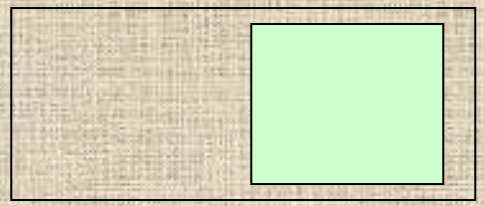


Máscara 1

Difusión de pozo

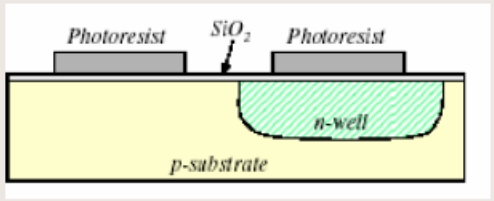
Pozo

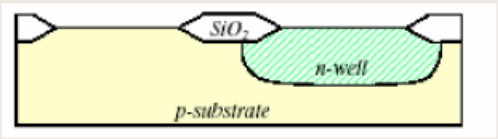




CMOS: etapas proceso fabricación

Define las regiones activas donde se van a colocar los dispositivos

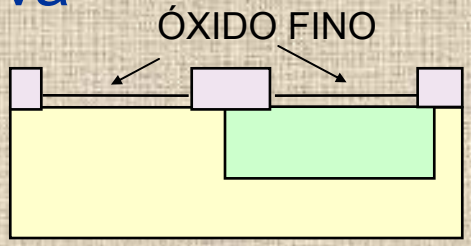


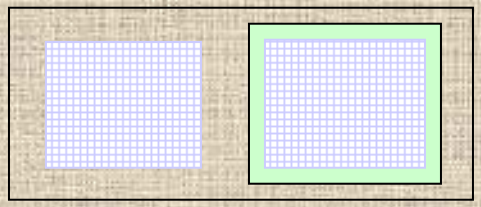


Máscara 2

Definición de áreas activas

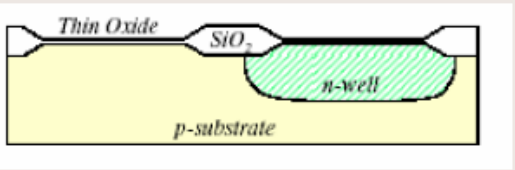
Área activa

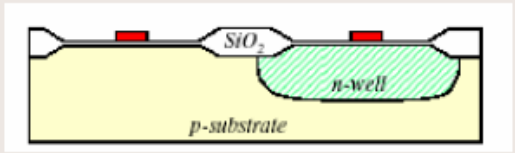


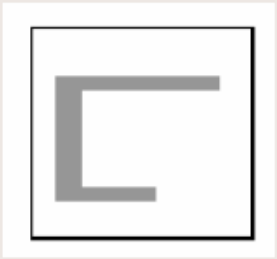


CMOS: etapas proceso fabricación

Se deposita el polisilicio de puerta



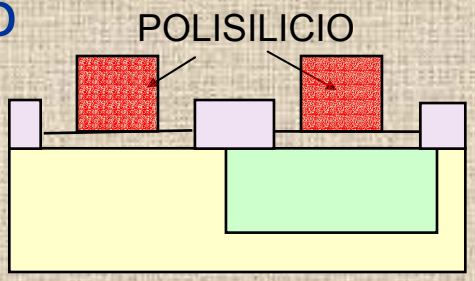


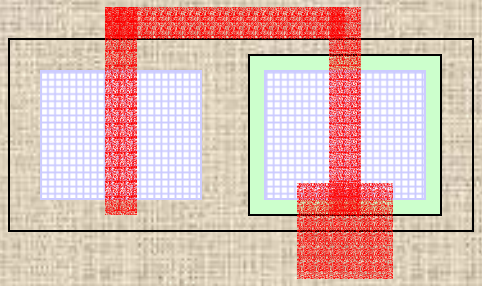


Máscara 3

Definición de las puertas

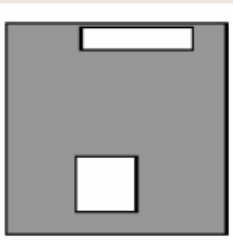
Polisilicio

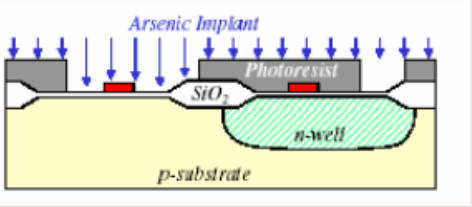


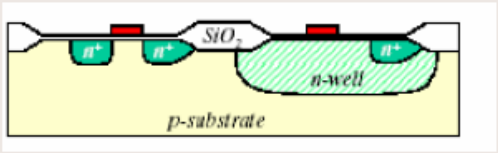


CMOS: etapas proceso fabricación

Se crea la fuente y el drenador de los dispositivos n



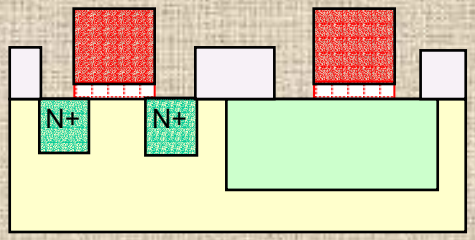


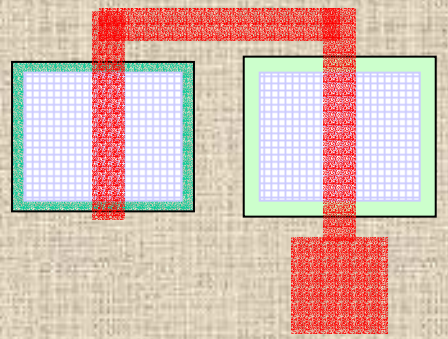


Máscara 4

Difusión n+
MOS canal N

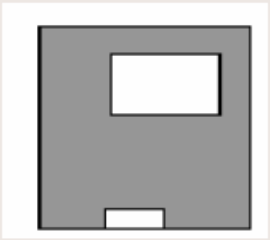
Implante N+

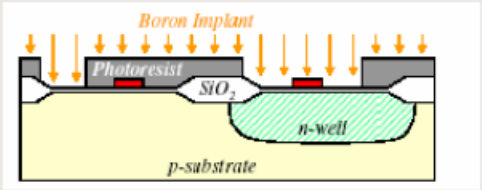


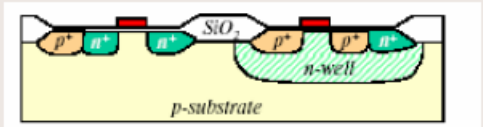


CMOS: etapas proceso fabricación

Se crea la fuente y el drenador de los dispositivos p



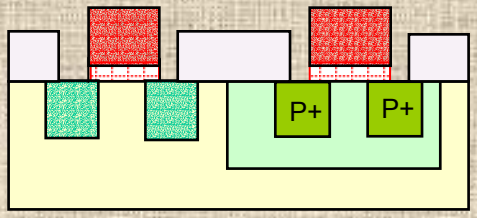


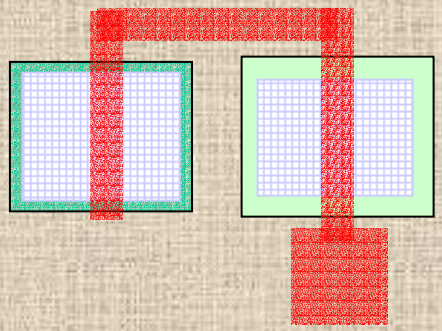


Máscara 5

Difusión p+
MOS canal P

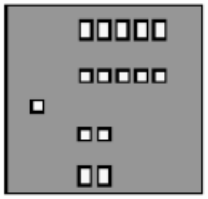
Implante P+

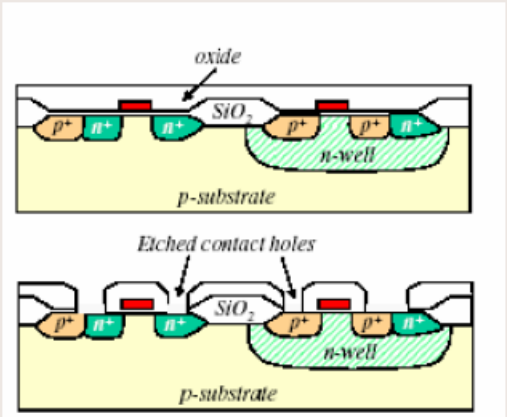




CMOS: etapas proceso fabricación

Determina las posiciones donde van los contactos

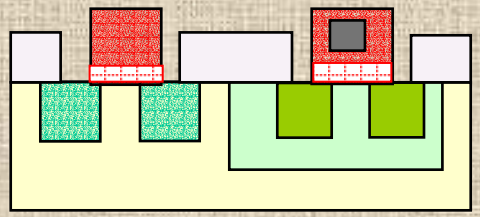


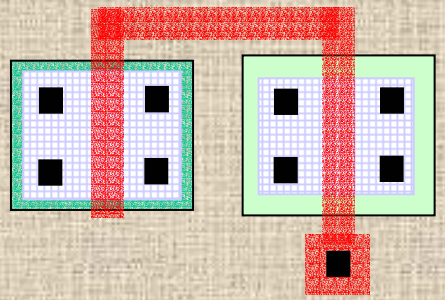


Máscara 6

Perforaciones de contacto

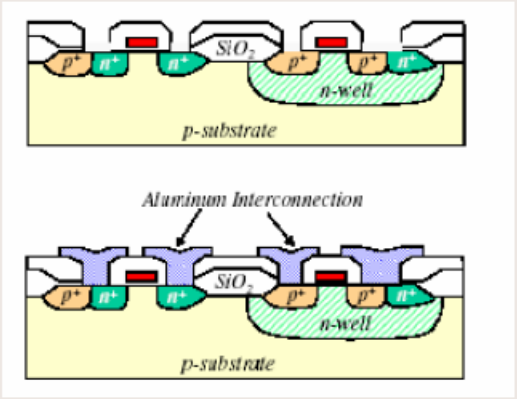
Contactos





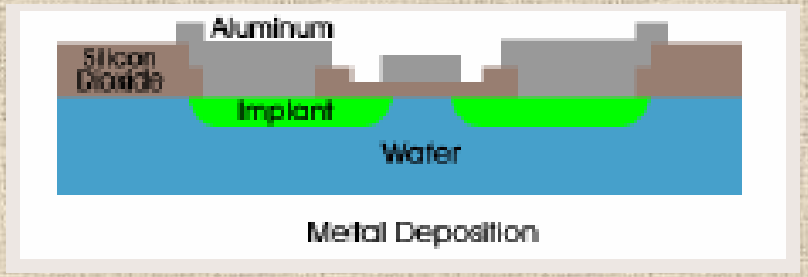
CMOS: etapas proceso fabricación

Determina las posiciones donde van las interconexiones

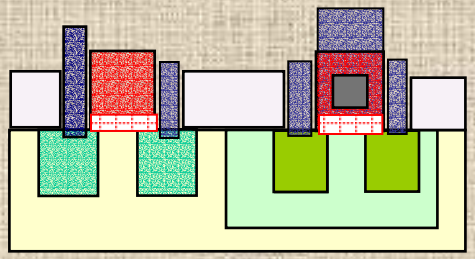


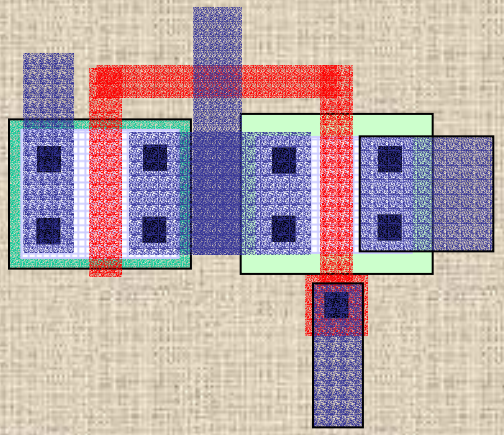
Máscara 7

Metalización

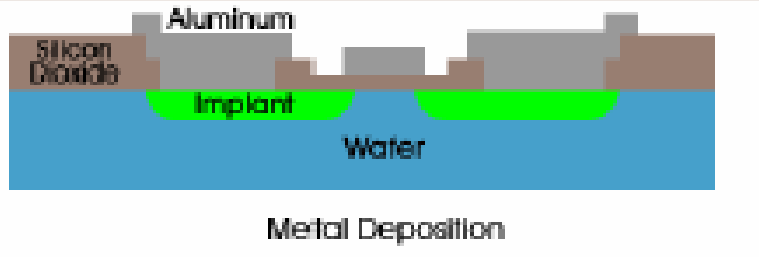


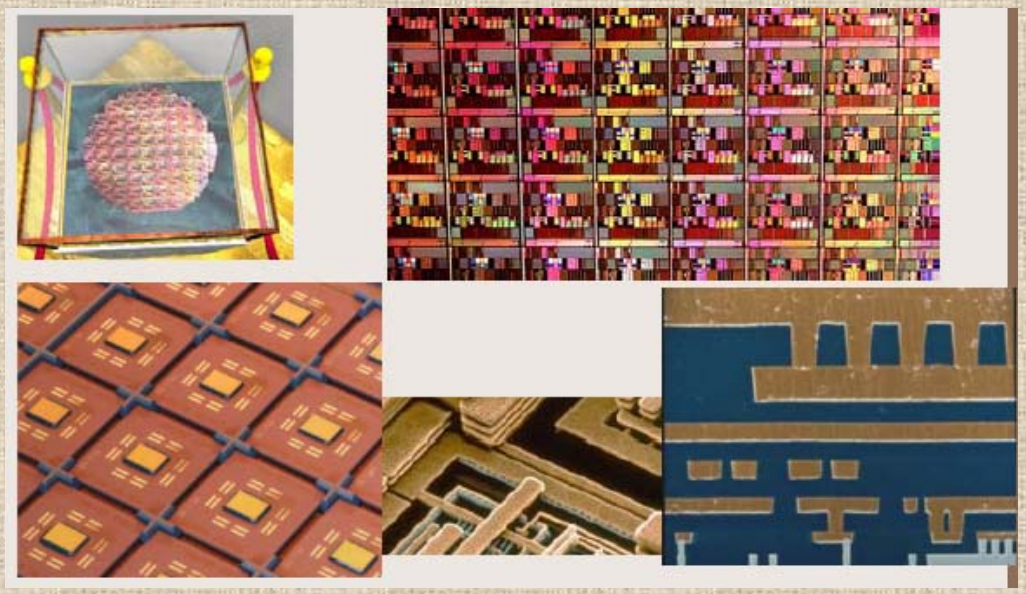
Metal





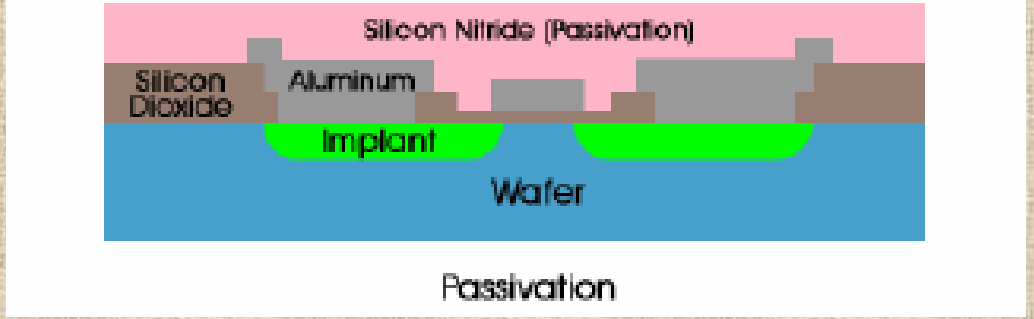
Máscara 7 Metalización



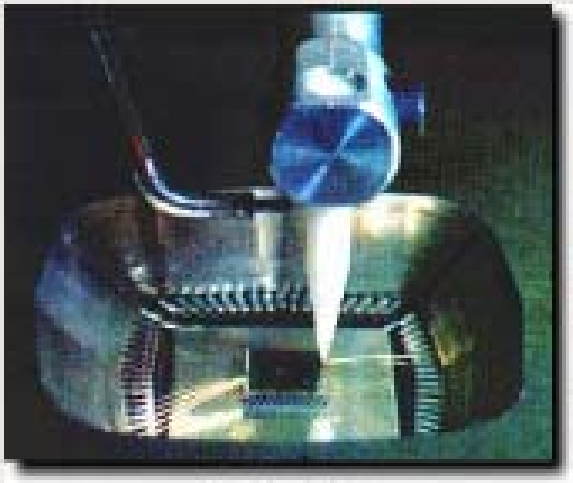


Máscara 8

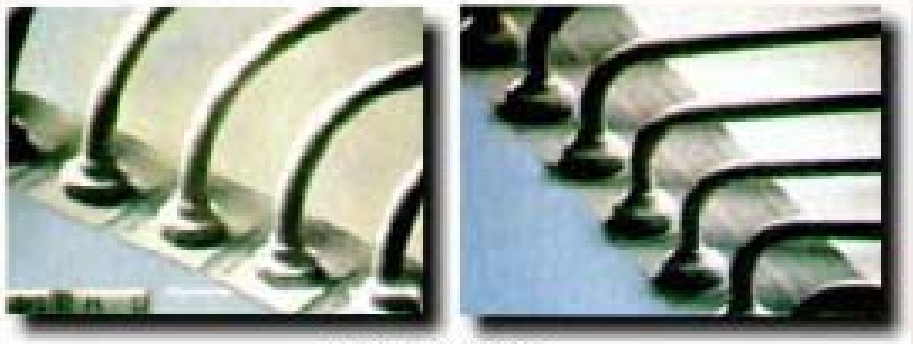
Pasivación



Conexionado (micro soldaduras)



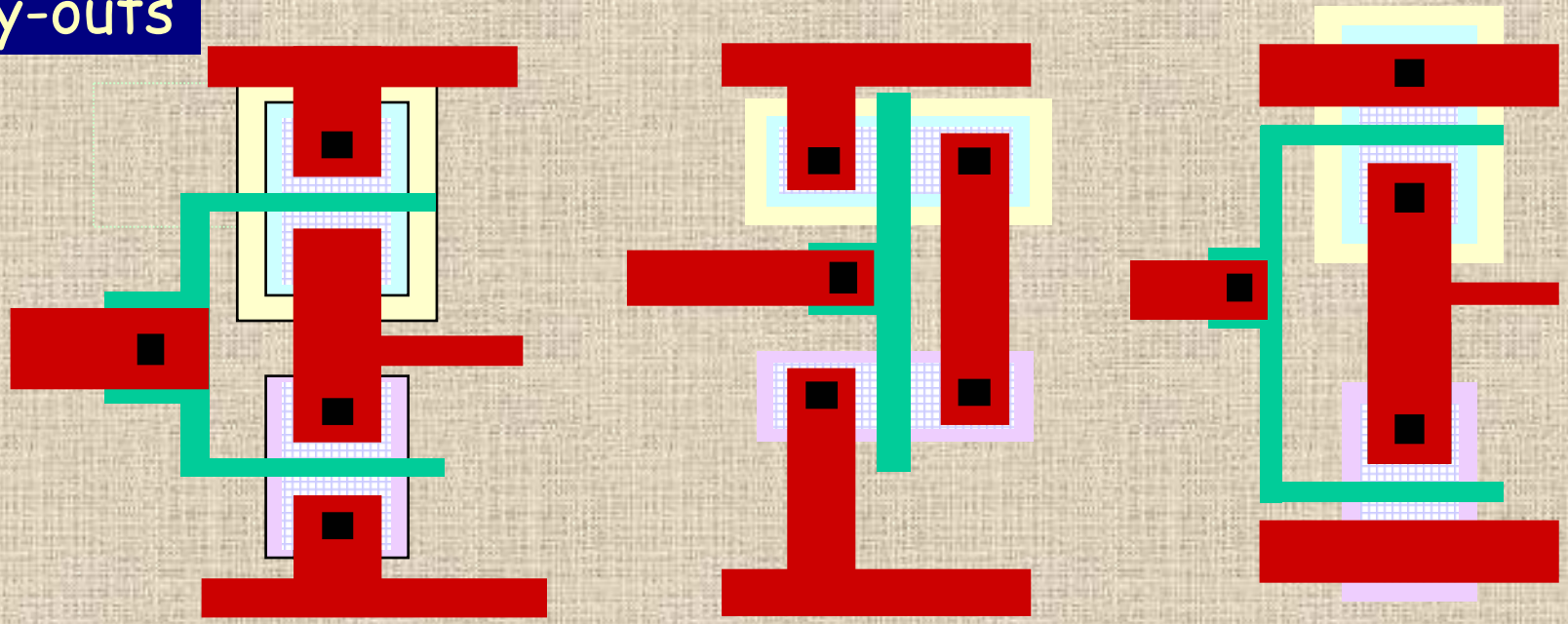
Wire Bonding
(Kulicke & Soffa Industries, Inc.)

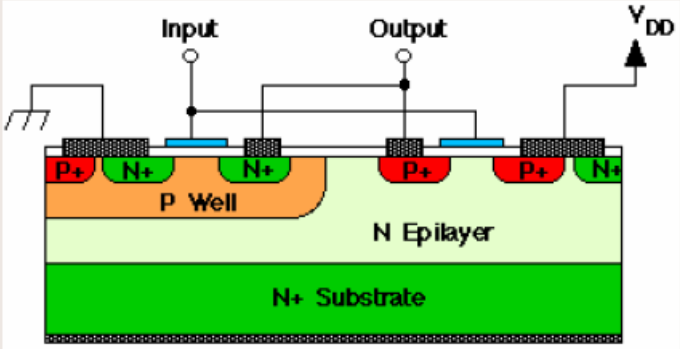


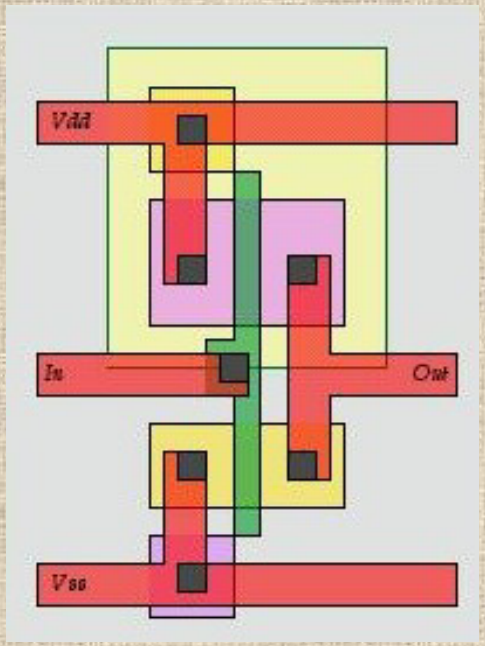
Wire Bonding
(Kaijo Corporation)

Die Lead Frame Attachment
(Ablestik)

Lay-outs

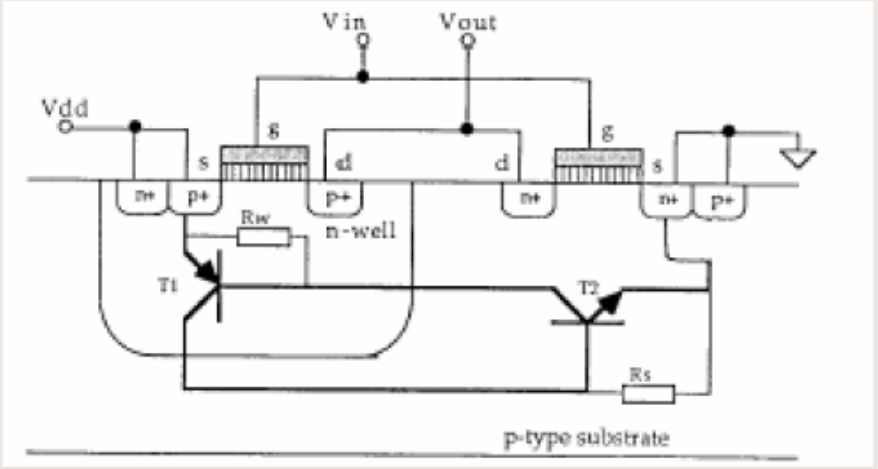



Input
Output
Y_{DD}
P+
N+
N+
P+
P+
N+
P Well
N Epilayer
N+ Substrate

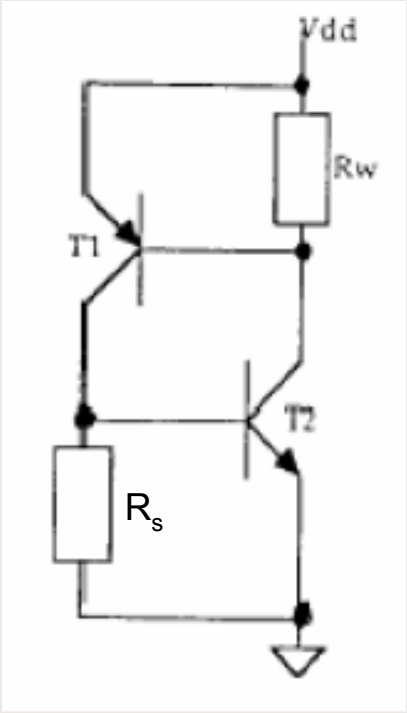

Vdd
In
Out
Vss

Latch-up

Generación de un camino de baja impedancia entre alimentación y tierra en un CI CMOS debido a la formación de transistores bipolares parásitos.



T1 y T2 conforman un tiristor



Valores elevados de Rs y Rw provocan la conducción de T1 y T2, la realimentación positiva intrínseca provoca un cortocircuito permanente entre V_{dd} y masa ⇒ LATCH-UP.

Precauciones

Aumento número de contactos pozo y sustrato. Proximidad a las fuentes de conexión

Aumento de la distancia entre dispositivos P y N

Anillos de guarda

Reducción de la resistividad de sustrato y pozo

Minimización de la ganancia de los transistores parásitos

Diseño de circuitos electrónicos

- especificación circuito
- Concepción y diseño
  - definición arquitectura
  - verificación funcional
  - diseño lógico y verificación
  - diseño circuital y verificación
- prototipos
- ensayo, verificación caracterización
- Fabricación en serie

Diseño Circuital y verificación

Diseño a nivel transistores

Dimensionamiento transistores

Simulación eléctrica pre lay-out

Layout y verificación reglas

Extracción del circuito

Simulación eléctrica post lay-out